EUROQUARTZ

GDW64 LVDS VCXO

11.4 x 9.6 x 4.7mm 6 pad SMD

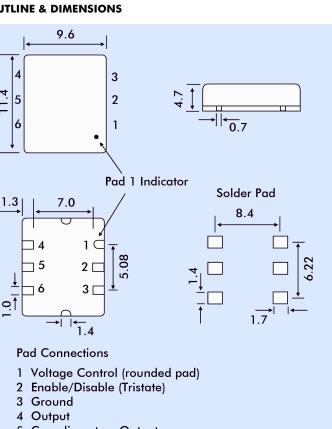
- Frequency range 750kHz to 800MHz .
- **LVDS Output**
- Supply Voltage 3.3 VDC
- Phase jitter 2.35ps typical
- Pull range from ±30ppm to ±150ppm

DESCRIPTION

GDW64 VCXOs are packaged in a 6 pad 11.4 x 9.6mm SMD package. Typical phase jitter for GDW series VCXOs is 2.35ps. Output is LVDS. Applications include phase lock loop, SONET/ATM, set-top boxes, MPEG , audio/video modulation, video game consoles and HDTV.

SPECIFICATION

Frequency Range:	750kHz to 800.0MHz	
Supply Voltage:	3.3 VDC ±5%	
Output Logic:	LVDS	
RMS Period Jitter:	4.3ps typical	
Peak to Peak Jitter:	27.0ps typical	
Phase Jitter:	2.35ps typical	
Initial Frequency Accuracy:	Tune to the nominal frequency with Vc= 1.65 ±0.2VDC	
Output Voltage HIGH (1):	1.4 Volts typical	
Output Voltage LOW (0):	1.1 Volts typical	
Pulling Range:	From ±30ppm to ±150ppm	
Control Voltage Range:	1.65 ±1.35 Volts	
Temperature Stability:	See table	
Output Load:	50 Ω into Vdd or Thevenin equiv.	
Rise/Fall Times:	0.5ns typ., 0.7ns max. 20% Vdd to 80% Vdd	
Duty Cycle:	50% ±5%	
	(Measured at Vdd-1.3V)	
Start-up Time:	10ms maximum, 5ms typical	
Current Consumption:	55mA typical, 60mA maximum (At 202.50MHz)	
Static Discharge Protection:	2kV maximum	
Storage Temperature:	-55° to +150°C	
Ageing:	±2ppm per year maximum	
Enable/Disable:	See table	
RoHS Status:	Fully compliant or non compliant	



- 5 Complimentary Output
- 6 Supply Voltage

FREQUENCY STABILITY

Stability Code	Stability ±ppm	Temp. Range
А	25	0°~+70°C
В	50	0°~+70°C
С	100	0°~+70°C
D	25	-40°~+85°C
E	50	-40°~+85°C
F	100	-40°~+85°C
If non-standard frequency stability is required		

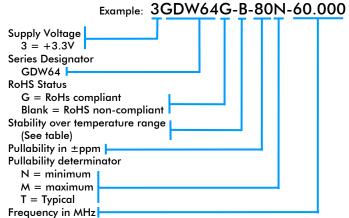
Use 'l' followed by stability, i.e. 120 for ±20ppm

ENABLE/DISABLE FUNCTION

Tristate Pad Status	Output Status
Not connected Below 0.3Vdd (Ref. to ground)	LVDS and Complimentary LVDS enabled Both outputs are disabled (high impedance)
Above 0.7Vdd (Ref. to ground)	Both outputs are enabled

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PART NUMBERING



750.0kHz to 800.0MHz



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OUTLINE & DIMENSIONS